order of a few percents when $b/b' = 0.5$. Note that formula (19) is also applicable to MIC disk resonators of smaller diameter, such as are used in the traditional Y-junction MIC circulators.

VI. Conclusions

A study has been presented of the $TM_{0,n,0}$ modes in ferrite MIC disk resonators of large diameter magnetized perpendicularly to the ground plane. Fringing-field effects have been included in the analysis via a semiempirical equivalent model. A fringing-field parameter b/b' has been introduced which allows one to predict the correct mode chart of a disk resonator. Numerical values of b/b' have been determined at C and X band for a dc magnetic field ranging from 0 to 3.5 kOe. Transition points have been found on the mode chart of the resonator where EGW modes transform into FV modes. Fringing fields are found to be responsible for the existence of these points. Finally, the ratio of the fringing field's power to the RF power stored within the ferrite under the strip conductor is determined as a function of the fringing-field parameter b/b'.

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Experimental Measurement of Microstrip Transistor-Package Parasitic Reactances

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***Abstract*—A resonance method of measurement is described for the determination of the parasitic reactances of a microwave transistor package mounted in microstrip. Results for two types of package obtained from normal-sized and from scaled-up models are presented. The influence of the parasitics on the characteristics of a typical microwave FET chip is briefly discussed.**

I. Introduction

The parasitic reactances associated with the package or mounting can seriously limit the performance of a microwave semiconductor device and need to be accurately known for good circuit and device modeling. Some diode packages in coaxial mounts, such as the S4 have been examined thoroughly [1], [2], but relatively sparse data are available on packages for microstrip application [3], [12]. The rapid advance in the performance of gallium arsenide FET's highlights the need for the accurate characterization and improvement of packages and mountings suitable for hybrid MIC's. In this paper two types of transistor packages will be considered, the leadless inverted device (LID) and the S2 package proposed by James *et al.* [4].

Previous papers [5]–[7] have described the measurement of the small reactances and susceptances of microstrip junctions and discontinuities, using a resonance technique and a close approach to a substitution procedure. In this procedure the change in resonant frequency is observed when the unknown element is introduced into a microstrip resonant circuit, only light coupling through noncritical connections being required for accurate determination of resonance. This method has the advantage of largely avoiding the problems entailed in the measurement of microstrip circuits through a coaxial-to-microstrip transition. While this approach often cannot be directly used for active devices, due to the low-circuit Q-factor that would result, it can be usefully applied to the study of the package parasitics. In addition to examining normal-sized packages with the active element appropriately disabled or disconnected, the method has been used to study scaled-up models of the package and circuit, Stycast material of the correct permittivity being employed in place of the ceramics of the package and circuit substrate. This is a quick and accurate method

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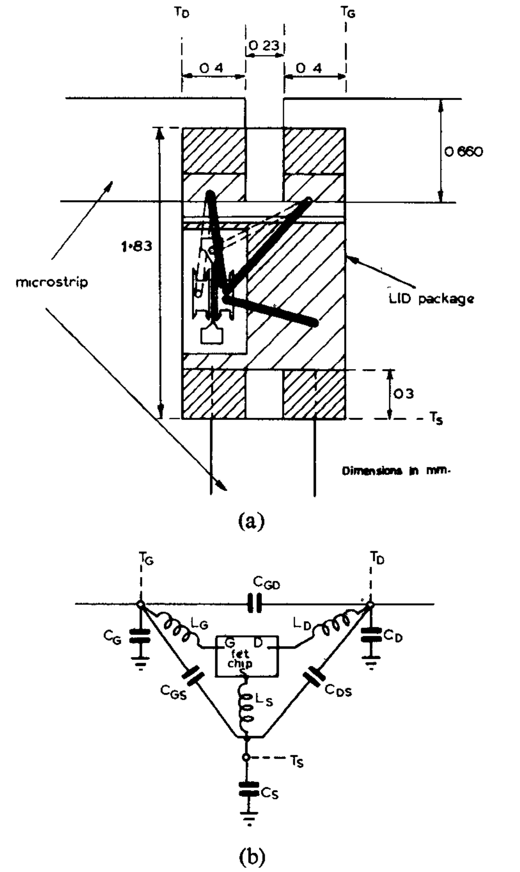


Fig. 1. (a) Bottom view of specially bonded normal size LID mounted on a 0.660-mm microstrip. T_G, T_D, and T_S are taken for the reference planes. Note: in a normal device, and the X8 model, the drain and gate wires were in the positions shown by the broken lines. (b) Equivalent circuit of LID package mounted as in Fig. 1(a) Note: C_G, C_D, and C_S include the microstrip capacitances under the contact pads of LID.

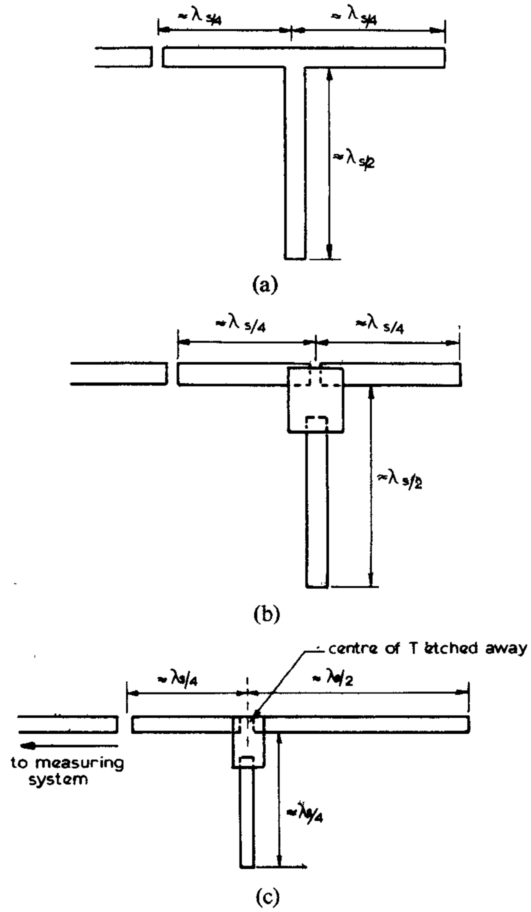


Fig. 2. (a) Reference T-junction resonator. (b) Configuration for determining $(L_G + L_D)$. (c) Test section for measuring $(L_G + L_S)$; for measuring $(L_D + L_S)$ the mirror image of the above is used.

for examining the effect of rearranging bonds and connections, as changes in both can be made without removing the scaled-up package from the microstrip circuit. Quite small effects can be directly observed without the variabilities inherent if the package must be removed and replaced. An important general advantage of the technique described is that the package may be evaluated in a mounting configuration close to that in which the device will be employed.

II. The LID Package

The general features of the LID package are shown in Fig. 1(a) which shows the arrangement of a typical FET chip and the bond wires. The package is normally mounted on the upper surface of a microstrip circuit and is connected to three 50-Ω microstrip lines on 0.660-mm alumina. Also indicated are the reference planes for the assumed equivalent circuit of Fig. 1(b).

A. LID Inductance

A modified device is employed with the three bonds connected to the same point as indicated in Fig. 1(a). When mounted, the device forms a modified microstrip T junction which may be characterized by the method of [7]. $(L_G + L_D)$ is first determined employing the configuration of Fig. 2(b), where the "top" of the T forms a half-wave resonator with L_G and L_D at the position of the current maximum. The stem of the T is approximately half-wave in length and presents a high impedance which is connected at a low-impedance point; thus L_S, etc., have very little effect on the resonance. In order to gain the advantages of the substitution method, a reference T-junction resonator was first measured [Fig. 2(a)]. Using the equivalent-circuit values of [7] for the end and gap effect and also the T junction in conjunction with the physical length of the resonator, the microstrip velocity was determined for the measured resonant frequency. The junction of the T was then etched away and the LID package mounted, and the resonant frequency redetermined, enabling $(L_G + L_D)$ to be found. The effect of the capacitances C_G, C_D, and C_S is small, as they are virtually at a voltage zero. If necessary, their presence can be allowed for. If the stem of the T does not present an ideal open circuit to the top section, the method relies on the symmetry of the T configuration. However, it can be shown that moderate departures (e.g., 5°–10° of electrical length) from this condition have only a slight effect and can be taken into account if necessary.

By using an L-shaped resonator [Fig. 2(c)], again with a $\lambda/2$ arm to terminate the third port in an effective open circuit, the values of $(L_G + L_S)$, and in a similar way

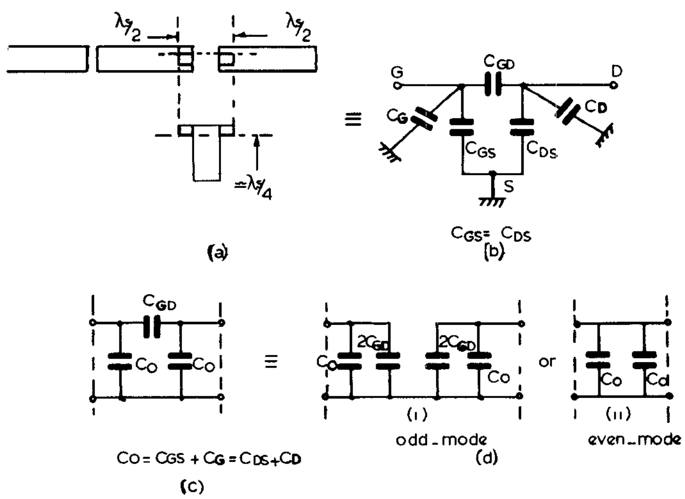


Fig. 3. The capacitive π-network.

$(L_D + L_S)$, could be found, the latter being evaluated from the measurements made on a mirror-image circuit of the former. Similar tests were performed on the X8 scaled-up model, but in one of these tests three source bond-wires were used and then two removed (while the package was *in situ*) to observe the effect of using more than one wire to reduce the inductance.

The normal-size tests were conducted on 50-Ω test circuits on 0.66-mm-thick alumina substrates while the scaled tests were performed on 5.29-mm-thick Stycast material having relative permittivity of 10.

B. Capacitance Measurements

The capacitances of an empty package were initially measured using the General Radio type 1616—a three-terminal low-frequency capacitance bridge. They were then measured at microwave frequencies. As the device was not mounted in microstrip for the low-frequency measurements, the capacitance value can differ from that obtained under normal mounting conditions. The resonance technique used for the microwave measurements is based on the capacitive π-network model for a gap in microstrip line [8]–[10].

The LID in the microstrip configuration of Fig. 3(a) has an equivalent circuit of Fig. 3(b) where the ground connection of the source pad is provided by the $\lambda/4$-line in Fig. 3(a). On resonating the circuit, the odd (lower) and even (higher) resonance frequencies (typically, 6.86 and 7.24 GHz) that correspond to the equivalent circuits of Fig. 3(d)(i) and (ii), respectively, were observed and used to evaluate the capacitances C_0 and $2C_{GD}$. As C_G or C_D cannot be physically separated from either C_{GS} or C_{DS}, C_0 and C_{GD} are the effective parasitic capacitances that appear at the package terminals when the package is mounted in microstrip. It can be shown that the length of the $\lambda/4$ line to the source contact-pads has only small influence on the capacitance values. For example, an error of (say) 10° in the electrical length of this line at 7 GHz would cause an error of 4 percent in the value of the capacitance C_0.

In Table I, results are shown for both the real-size and scaled-up LID. As the reference plane is taken at the edge of the package, the inductance values include the inductances of the lead wires and those of the package metallization.

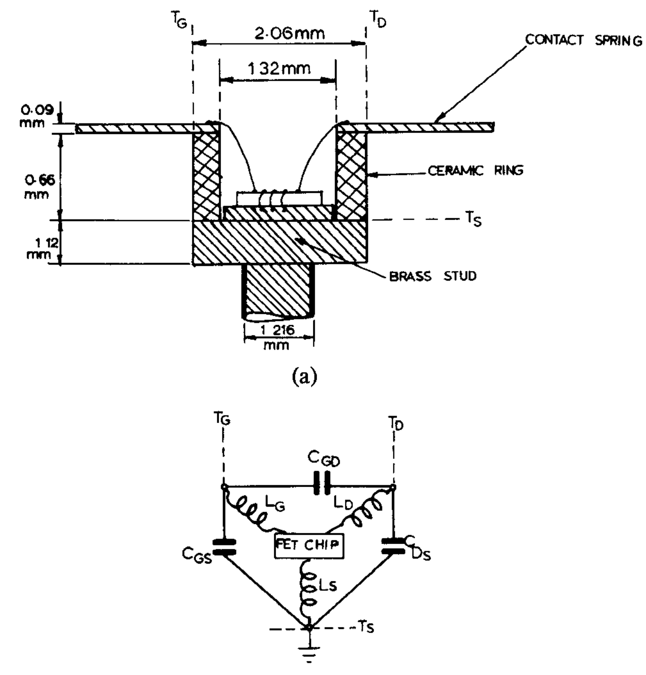


Fig. 4. (a) S2 package bond-wire layout. (b) S2 package equivalent circuit.

TABLE I
LID PACKAGE REACTANCE

Parameter	Normal size device		X8 Scaled model, values scaled to normal size	
	Measured value	Form of device	Measured value	Form of device
(1)* L_G,nH	0.66+	Standard GAT2 device with all leads bonded to source pad. One source bond wire.	0.68	X8 LID packaged with dummy chip. All leads bonded to source pad. One source bond wire.
(2)* L_D,nH	0.61+		0.54	
(3)* L_S,nH	0.760		0.76	
(4)* L_S,nH	-	-	0.65+	As above but 3 source bond wires.
(5)** C_{GD},pF	0.026	Empty LID package	0.023	X8 Empty LID package
(6)* C_{GD},pF	0.038+		-	
(7)** C_0,pF	0.038		0.037	
(8)* C_0,pF	0.104+		-	

* Measured at microwave frequencies.
** Measured at low frequencies.
\+ Values used in Section 4.

III. THE S2 (CRC) PACKAGE

A. Inductance Measurements

The S2 package, shown in Fig. 4, has a threaded stud that connects the source bond-wires to the ground plane of the microstrip line; therefore, unlike the LID, the source must always be grounded. Hence, the T- and L-shaped

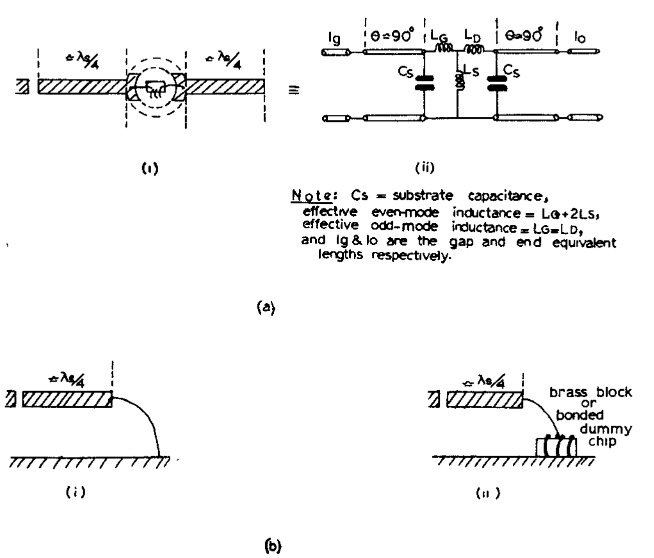


Fig. 5. Microstrip configuration for measuring S2 package inductances.

resonators previously used are not appropriate. The values of the three inductances of the bond-wires in Fig. 4(b) cannot be directly found separately, but may be deduced with reasonable accuracy by a series of experiments based on Fig. 5, where both or either of the normal-size and/or scaled-up models are used whenever convenient. Fig. 5(a)(i) shows the microstrip configuration used to determine L_G, L_D, and L_S. Fig. 5(a)(ii) is its electrical equivalent circuit. This circuit resonates in odd and even modes at frequencies corresponding to the effective value of inductance that terminates the $\lambda/4$ microstrip line. Using the known data for the end and gap effect [7], the values of L_G and L_S were calculated.

The method is usable only when the circuit is symmetrical. This condition was achieved by positioning of the dummy chip at the center of the package, thus making $L_G = L_D$, and then adjusting the lengths of the $\lambda/4$ lines in the scaled-up circuit. It can be shown that since the inductances being evaluated are at voltage nodes, slight asymmetry in the circuit causes very small error in the inductance values. The method has the advantage that it gives the overall inductance values including those due to the mutual inductance. However, it is not possible to separate the mutuals from the self-inductances. The results are given in Table II (L_1–L_3).

Further experiments to check the measured inductances of this package were carried out based on Fig. 5(b), where in Fig. 5(b)(i), a bond wire was connected from the gate terminal to the package stud and resonated in the microstrip system as shown. This wire is slightly longer than the normal gate bond-wire but of the same order of magnitude in inductance, the value of which is L_4. The inductance L_5 of the normal gate bond-wire was deduced from Fig. 5(b)(ii) in a scaled-up model, where a brass block of the same height as the semiconductor chip was used to shortcircuit the $\lambda/4$ line. The total inductance in this system is that of the bond wire plus that of the block which is of negligible value as compared to the former; so, we assume $L_G \simeq L_5$. A scaled-up dummy chip was also used to simulate the FET with the

TABLE II
THE MEASURED S2 PACKAGE REACTANCE

TYPE	PARAMETER DEFINITION	MEASURED VALUE Inductance in nH capacitance in pF
L_1	Inductance of gate bond-wire (L_G) from Fig. 5a; $L_G = L_D$.	0.525+
L_2	Inductance of gate bond wire and three source wire. ($L_G + L_S$)	0.768
L_3	Inductance of three source bond wires.	0.12+
L_{4A}	Inductance of short-circuiting wire in Fig. 5b (i)	0.595
L_{4B}		0.516*
L_5	Inductance of short-circuiting wire on brass-block (Fig. 5b (ii).	0.507
L_{6A}	Inductance with three source bond-wires bonded on top of the dummy chip (Fig. 5b (iii). ($L_G + L_S$)	0.63
L_{6B}		0.842*
L_7	Apparent inductance of three source bond wires $L_7 = (L_{6A} - L_5)$	0.123
L_8	Inductance of gate bond-wire and 2 source wires.	0.707
L_9	Apparent inductance of two source bond wires $L_9 = (L_8 - L_5)$	0.2
L_{10}	Inductance of gate bond-wire and one source bond wire.	0.761
L_{11}	Apparent inductance of one source wire $L_{11} = (L_{10} - L_5)$	0.256
C_{1A}	The gate to drain capacitance (C_{GD}) measured on the l.f. bridge @ 1kHz.	0.004
C_{1B}		0.003*+
C_2	The capacitance $C_0 = C_{GS} + C_G = C_{DS} + C_D$ measured at microwave frequencies (Fig.3)	0.097*+

* Values found from measurements on real-size models. Other values (without asterisks) are from scale-up models.
+ Values used in Section 4.

TABLE III
CHANGE IN INDUCTANCE WITH WIRE SPACING AND WITH USE OF RIBBON IN S2 PACKAGE

L, nH	COMMENTS / WIRE SPACING	1.0	1.5	2.5	3.5
L_1	Inductance of bond wire on a brass dummy chip.	0.476	-	-	-
L_2	Inductance of three source bond-wires	0.178	0.166	0.141	0.108
L_3	Inductance of two source bond wires.	0.195	0.194	0.156	0.115
L_4	Inductance of one source bond wire.	0.274	-	-	-
L_5	Inductance of copper ribbon of width = 2.5 mm.	0.094	-	-	-
L_6	Inductance of copper ribbon of width 5mm	0.036	-	-	-

Note: All given figures are scaled-down values.

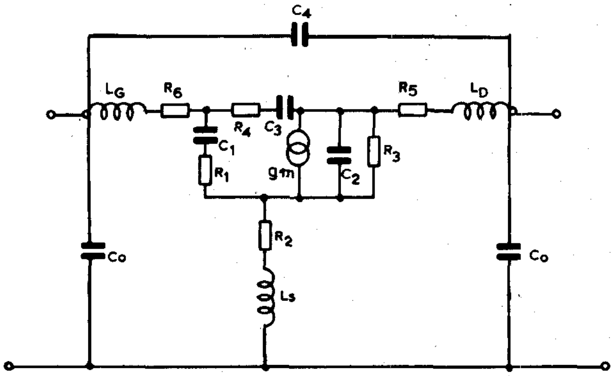
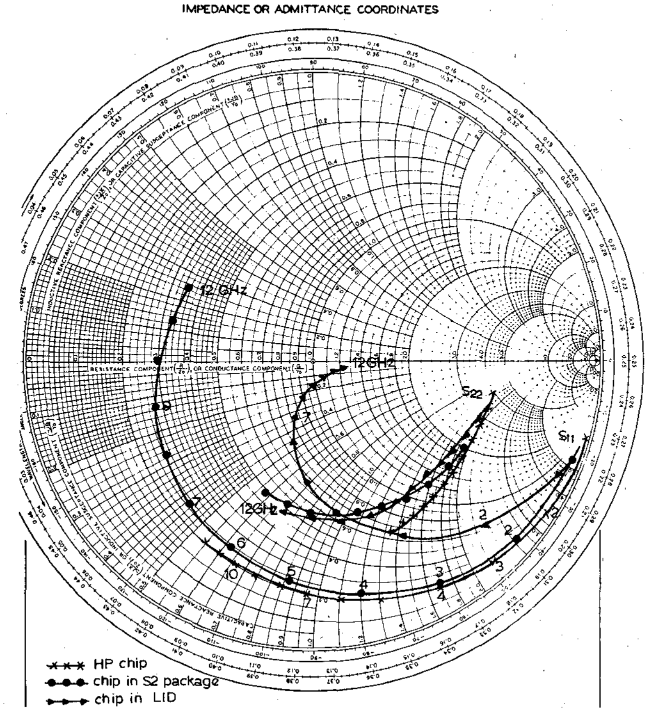
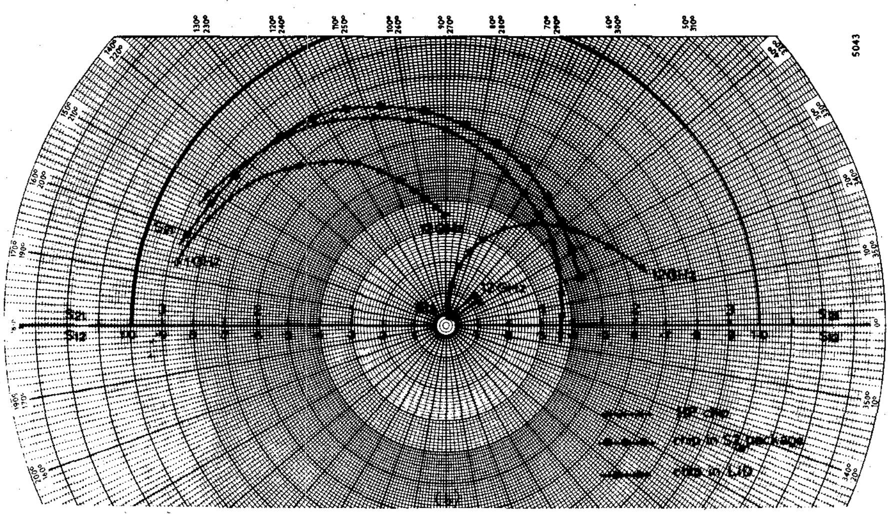


Fig. 6. Equivalent circuit of the packaged FET. $R_1 = 6.5$; $R_2 = 3.7$; $R_3 = 192$; $R_4 = 658$; $C_1 = 0.5$; $C_2 = 0.2$; $C_3 = 0.014$; $g_{m0} = 43$; $g_m = g_{m0}e^{-j\omega\tau_0}$; $\tau_0 = 5$ ps; $R_5 = R_6 = 0$. Resistance in ohms, capacitances in picofarads. C_0, C_4, L_G, L_D, and L_S taken from the package measurements (Tables I and II). Other values from [11].

gate and source bond-wires bonded on the same pad [as in Fig. 4(a)], the total inductance being $L_{6A} = (L_G + L_S)$. A standard FET (bonded at Plessey Co. Ltd., Towcester) was used in a real-size model for the same purpose, but with the drain bond-wires terminated on a microstrip line of length $\simeq\lambda/2$ to present a near open-circuit at the drain end on the



(a)



(b)

Fig. 7. (a) Effect of package parasitics on chip S-parameters (S_{11} and S_{22}). (b) Effect of package parasitics on chip S-parameters (S_{12} and S_{21}).

chip. The resulting inductance value $L_{6B} = (L_G + L_S)$ is seen to agree within an acceptable limit with L_2 from Fig. 5(a).

To show the effect of using more than one source bond-wire, after obtaining L_{6A} [from Fig. 5(b)(ii)], the number of wires was reduced by plucking them off one by one while the package was in position. The results (L_8–L_{11}) given in Table II show a reduction in the source inductance with an increase in the number of wires. Experiments were also conducted on the same circuit to show the effect of various spacings of the source bond-wires and also of the effect of conducting ribbon bonds on the source inductance. The results are shown in Table III.

It can be inferred that the changes seen in measuring the inductance L_{6A}, L_8, and L_{10} are predominantly due to the change in L_S, but it should be noted that the measurement is in terms of $(L_G + L_S)$.

B. Capacitance Measurement

It was proposed to measure the S2 capacitances C_{GD}, C_{GS}, and C_{DS} using the same microwave method as used for the LID capacitances. However, due to the low value of C_{GD}, combined with low Q-factor of microstrip, only a single resonance was observed as would be expected from the value in Table II (C_{1B}). The low-frequency capacitance value of C_{GD} was thus used, whereas C_{GS} and C_{DS} were calculated from the observed resonance. The obtained values for these capacitances are in Table II.

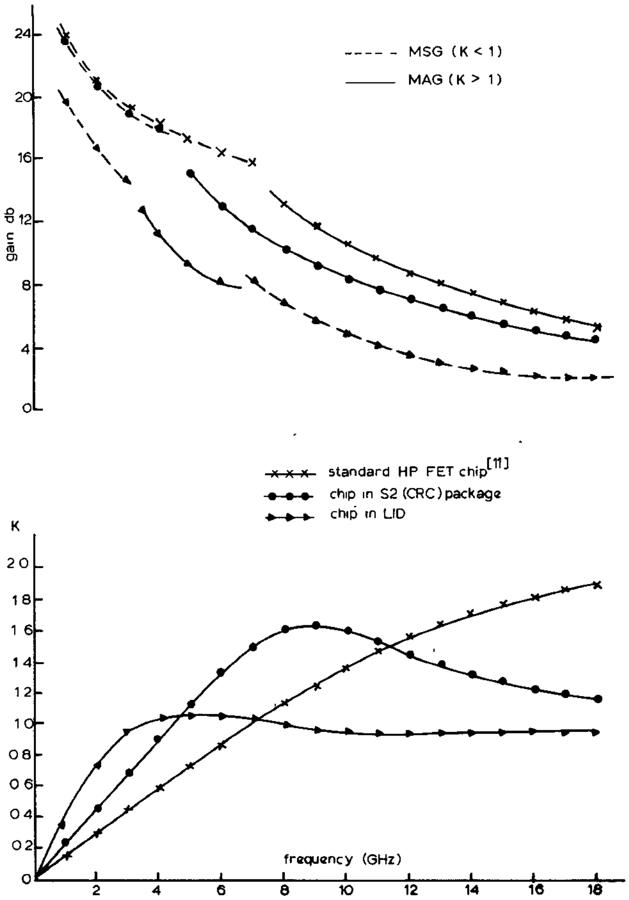


Fig. 8. Gain and stability factor (K).

IV. Effects of the Measured Package Parasitic Reactances on FET Chip Characteristics

To demonstrate the effect of the measured package reactances on chip performance, the Hewlett-Packard 1-μm MESFET chip [11], with the parameters shown in Fig. 6 was taken and the values for the parasitics (indicated in Tables I and II) added using the Z-, Y-, and S-matrices. The overall S-parameters, gain (MSG and MAG) and stability factor (K) were computed for the chip in the two types of package. The results are given in Figs. 7 and 8. Further analysis using this computation showed that most of the effects on the chip characteristics are due to L_S and C_{GD}.

V. Conclusions

a) The resonance method has been shown capable of accurately measuring very small package inductances and capacitances at microwave frequencies with the package mounted in a configuration similar to that of the circuit normally used.

b) From Tables I–III, it is seen that there is a reasonable agreement between the results obtained from the real-size and scaled-up models. This gives confidence in using scaled-up models, especially in cases where real-size devices are too small for easy handling and where quick changes in circuit configuration are necessary.

c) The results have been used to show the improvement in the performance of a typical chip embedded in the S2-type package (as compared to the LID package) in terms of broad-band matching (S_{11} and S_{22} of Fig. 7). The improvements stem from reduced values of both feedback capacitance C_{GD} and the source lead inductance L_S. Thus, apart from the higher gain obtained in the S2-type package, the device remains potentially stable over a broader band of frequency.

Acknowledgment

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